EFFECT OF TUNNEL RESISTANCE IN THE STRONG TUNNELING REGIME ON THE CONDUCTANCE OF THE SINGLE ELECTRON TRANSISTORS FABRICATED USING FOCUSED ION BEAM ETCHING

P. Santosh Kumar Karre* and Paul. L. Bergstrom
Multi Scale Technologies Institute (MuSTI), Department of Electrical and Computer Engineering,
Michigan Technological University, Houghton, Michigan-49931, USA.

Govind Mallick and Shashi P. Karna
US Army Research Laboratory, Weapons & Materials Directorate, ATTN: AMSRD-ARL-WM, Bldg. 4600, Aberdeen Proving Ground, MD 21005-5069, USA.

ABSTRACT

Ultra light and portable nano systems with integrated functionalities of sensing, data acquisition, data processing and communications will improve the effectiveness of electronic systems and potentially improve the decision making time in the battle field for the Land Warrior. Nanoelectronic devices form the building blocks of nanoscaled systems and require innovative technologies for their realization. The single electron transistor (SET) is a novel class of nano transistor which operates using quantum mechanical processes, Single electron transistors can be fabricated using methods like AFM nano oxidation, *e*-beam lithography, or shadow mask evaporation. Focused Ion Beam (FIB) based fabrication of SET devices is a novel method to produce SETs. SET based nano systems will enable potentially novel embedded applications to the Future Force Warriors (FFW) and Future Combat Systems (FCS). We report on the characterization of multiple SET devices in the strong tunneling regime. The effect of the magnitude of tunnel resistance on the conductance of the SET in the strong tunneling regime is studied and the experimental data is in close correlation with theory of strong tunneling. Characterization and understanding the SET device characteristics are vital for the realization of integrated nano scaled systems.

INTRODUCTION

Single electron transistor (SET) devices have device dimensions in the nano scale range and use quantum effects for their operation. SETs are a prime candidate for future nano scaled systems because of their low power consumption, their high speed of operation, smaller device area, their promising capability to integrate in ultra-high density memories, and their ability to sense minute charge fluctuations. SET devices have been fabricated using various material systems such as Si/SiO [Takahashi et al., 1995], GaAs [Nakazato et al., 1992], and carbon nanotube [Park et al., 2001] systems. Focused Ion Beam (FIB) based fabrication is a novel method to fabricate SETs. Focused Ion Beam (FIB) etching has proven to be a very useful tool in the fabrication of nanoscaled structures [Petit et al., 2005]. The tunnel resistance of the SET device should be greater than the quantum of resistance to confine electrons on the quantum island, and the charging energy of the device should be greater than the thermal energy to observe coulomb oscillations. If the tunnel resistance of the SET is less than the quantum of resistance then the SET operates in the strong tunneling regime. The differences in the characteristics of multiple SET devices arise from the size difference of the conducting island and the difference in magnitude of tunnel resistance. Single Electron Transistors (SET) were fabricated using FIB etching technology. The quantum island size of the SET devices were less than 90nm, and the tunnel junction width of the SET devices were less than 30nm. The initial characteristics of the devices at room temperature show that the coulomb oscillations are suppressed, as expected for this island size in a metallic system. The conductance of SET displays an asymptotic behavior, which is attributed to the operation of SET in the strong tunnel regime, and to operation at room temperature. Higher conductance is displayed by devices having lower tunnel resistance, which is in accordance with the theory of strong tunneling in SET.

I. DEVICE FABRICATION

The SET device is fabricated using FIB etching technology, where highly focused beams of energetic Ga^+ ions are used to ablate a pattern in the substrate. Single Electron Transistors are fabricated in a series of process steps utilizing high beam currents and low beam currents available on the FIB. Lower beam currents are used to fabricate nano scaled structures, which require smaller energy doses, whereas higher beam currents are used to realize the micro scaled structures. The fabrication of the SET using FIB etching is explained elsewhere [Karre, et al., 2006]. A 150nm thin film of Al_2O_3 is deposited on a

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
01 NOV 2006	**N/A**	**-**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Effect Of Tunnel Resistance In The Strong Tunneling Regime On The Conductance Of The Single Electron Transistors Fabricated Using Focused Ion Beam Etching	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **Multi Scale Technologies Institute (MuSTI), Department of Electrical and Computer Engineering, Michigan Technological University, Houghton, Michigan-49931, USA**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release, distribution unlimited

13. SUPPLEMENTARY NOTES
See also ADM002075., The original document contains color images.

14. ABSTRACT

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**	**UU**	**5**	

clean silicon wafer using radio frequency (RF) sputter deposition in a Perkin Elmer 2400-8J parallel plate sputtering system. The Al_2O_3 is used as a high quality isolating layer. Following the deposition of Al_2O_3, a 50nm thin layer of Ni is deposited using the same system for the fabrication of quantum islands and device electrodes. SET devices were fabricated to have different tunnel widths. The tunnel widths of the device can be precisely controlled using FIB etching. The tunnel widths of the device impact the tunnel resistances of the tunnel junctions. The island size of the device can be controlled in the device fabrication process. Differences in the island size of the device results in different capacitances of the device. The SEM micrograph in Fig. 1 shows a SET device having a tunnel junction width of 20nm and a metallic nano island of diameter 60nm. The SEM micrograph of a SET device having a tunnel junction width of 30nm and a metallic island of diameter 90nm is shown in Fig 2. The conductance of the SET device in the strong tunneling regime at room temperature can be explained using Equation 1, where the conductance of the device is dependent on both the tunnel resistances of the device and the charging energy of the device [Chouvaev et al., 1999]. For a particular value of the charging energy of the device the conductance asymptotes will depend on the total resistance of the device. The higher the combined tunnel resistance of the device, the lower would be the conductance of the SET.

The combined resistance of the device can be calculated from the experimental data from the I-V characteristics of the device. The charging energy of the device is dependent on the total capacitance of the device, the following section deals with the calculation of the total capacitance of the device.

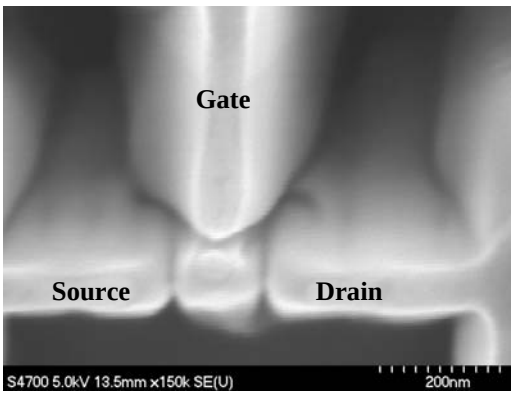

Figure 1: Full SEM plan view of a SET test device structure.

$$G(T) = \frac{1}{R_\Sigma}\left(1 - \frac{E_C}{3T} + \ldots\right) \qquad (1)$$

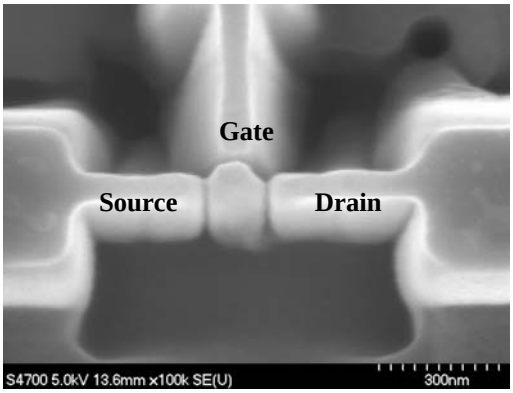

Figure 2: Magnified SEM view showing the active device area.

II. DEVICE CAPACITANCE

The capacitance of the device is dependent on the island shape and the electrical environment in which the island is embedded. The conducting island is spherical in shape, and it is embedded in the dielectric material of Al_2O_3, which has a dielectric constant of 9.6 F/m. The capacitance of the island is given by $C = 4\pi\varepsilon\varepsilon_r r$, where C is the capacitance, ε_r is relative dielectric constant of the material, and r is the radius of the conducting island. The capacitance value obtained for the island is $C_{island} = 3.2x10^{-17} F$. The capacitance of the tunnel junction can be approximated by

$$C = 2\pi\varepsilon\sqrt{d^2 - 4a^2}\sum_{j=0}^{\alpha}(\coth[(j+1/2)\operatorname{arccosh}(d/2a)] - 1) \qquad (2)$$

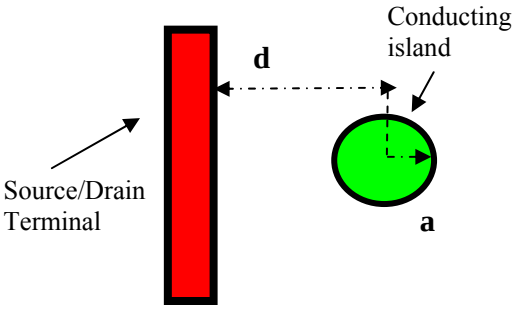

Figure 3: Capacitance between the quantum island and the terminal.

The tunnel junction is composed of a plane of metal on one side and a conducting island on the other side. The capacitance for such a structure is given by Equation (2), where a is the radius of the sphere, and d is the distance between the centre of the sphere and the metal sheet. The radius of the conducting island in one of the device is $a=30$ *nm*, and the distance $d=100$*nm*, taking the tunneling gap to be 20nm. The tunnel capacitance is given by $C_{TunnelJunction} = 0.104X10^{-18} F$. Since the tunnel

junction on the right is symmetrical and has the same tunneling gap, the tunnel junction capacitance on the right is also equals the above value $C_{TunnelJunction} = 0.104X10^{-18}F$

The gap between the gate and the conducting island is found to be ~20nm, and considering the gate terminal to be a plane sheet (The geometry is slightly different); the capacitance between the gate and the island is again equal to the capacitance of the tunnel junction. Hence the capacitance between the gate terminal and the conducting island is given by $C_{Gate-Island} = 0.104X10^{-18}F$. The approximate value of the capacitance of the device is the sum of all the capacitance including the parasitic capacitance, which is not included here. Hence, $C = 1.755x10^{-17}F$ for device 1 and $C = 4.804x10^{-17}F$ for device 2. For the device to operate at room temperature these capacitance values should be further reduced. The conductance of the device for variation in the tunnel resistances is calculated using Equation (1). The tunnel resistance is varied from 5KΩ to 25KΩ for a fixed value of charging energy of the system. The results of the variation of conductance due to the variation of the tunnel resistance are shown in the Fig 5. It is observed that for a smaller tunnel resistance, the conductance is high. With increase in the tunnel resistance the conductance of the SET decreases. The tunnel resistance of the SET can be changed by varying the tunnel junction width of the SET. The tunnel junction width of the SET can be precisely controlled in the FIB etching process. It is observed that the conductance is a strong function of the tunnel resistance and the conductance of the device decreases with the increase in the tunnel resistance of the device, which is in accordance with the theory of strong tunneling [Chouvaev et al., 1999].

III. DEVICE CHARACTERISTICS

The source drain characteristics of the fabricated SET at room temperature are shown in Fig. 5 and Fig. 6, respectively. The tunnel resistance of the SET was calculated from the I-V characteristics. These calculations indicate that the SET is operating in the strong tunneling regime, with a tunnel resistance comparable in magnitude to the quantum resistance. The tunnel resistance of the device with a 20nm tunnel junction width has a tunnel resistance of 5KΩ and the device with tunnel junction width of 30nm has a tunnel resistance of 22KΩ The tunnel resistance being comparable to the quantum of resistance results in a broadening and overlap of excited charge states, thus causing suppression of the single charge effects due to dissipation [Chouvaev et al., 1999]. The amplitude of the oscillations decay exponentially at higher temperatures [Golubev et al., 1997] demonstrating metallic characteristics. For the present case of strong tunneling at higher temperatures, the observed conductance reaches its asymptotic value as shown in Fig. 4 and Fig. 6. The device with the tunneling gap of 20nm had a tunnel resistance of 5KΩ. Hence, the conductance of the device is more than the conductance of the device with 30nm tunnel junction width and the tunnel resistance of 22kΩ. The differences in the island size also contribute to the difference in conductance, but the tunnel resistance of the device is a dominant factor affecting the conductance of the device. Hence, by varying the width of the tunnel junction in the fabrication process the tunnel resistance of the SET can be controlled in the FIB etching process.

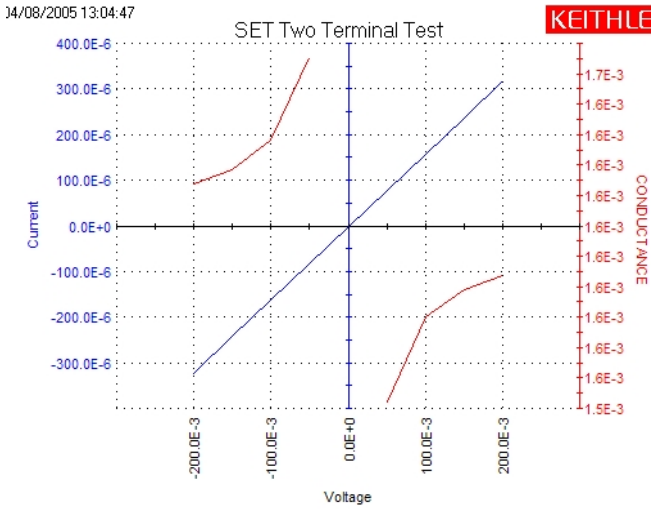

Figure 4: Output conductance graph of the SET device at room temperature for a fixed V_G.

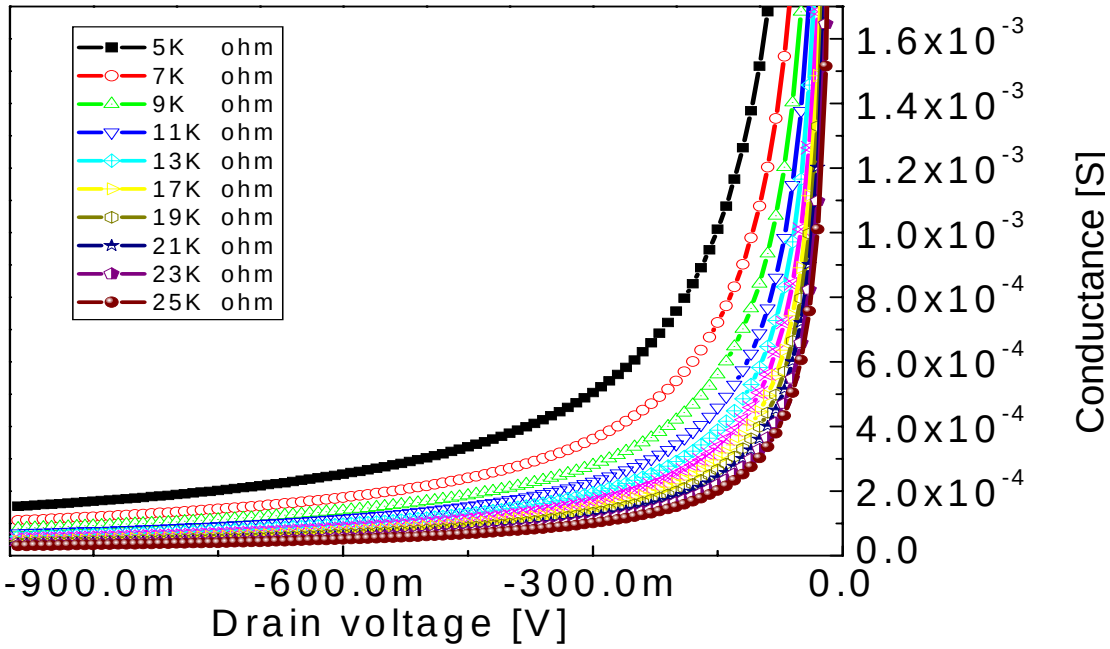

Figure 5: Theoretical calculations of the SET conductance with drain voltage.

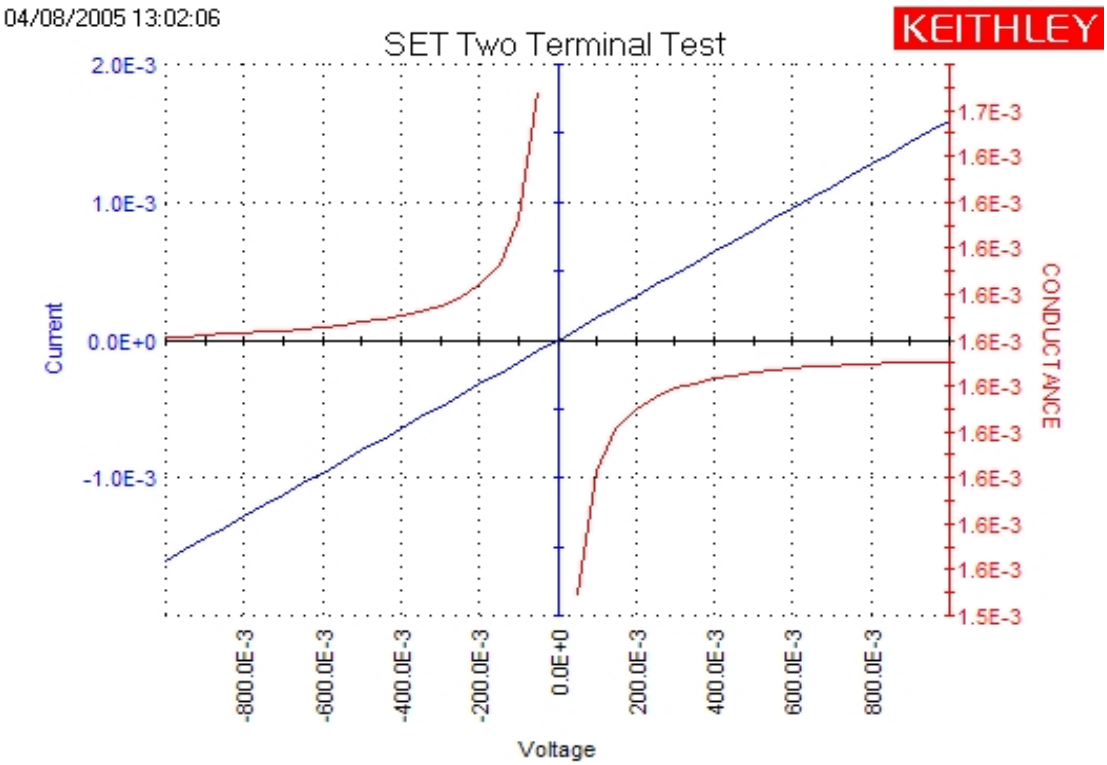

Figure 6: Output conductance graph of the SET device at Room temperature for a fixed V_G.

CONCLUSIONS

SET devices with different tunnel widths and different island sizes were fabricated using FIB etching. The differences in tunnel widths resulted in differences in tunnel resistances. The difference in the island size resulted in the difference in the capacitance of the device, hence, the charging energies. The conductance of the SET in the strong tunneling regime was calculated for different tunnel resistances. It was observed that the effect of tunnel resistance on the conductance of the SET was the dominant factor compared to the charging energy of the system. The experimental results obtained confirm the theoretical calculations of conductance of the SET in the strong tunneling regime. The fabricated devices had tunnel resistances of 5KΩ for a tunnel width of 20nm, and a tunnel resistance of 22kΩ for a tunnel width of 30nm. This difference in the fabricated structures resulted in differences in the device parameters, and therefore, in the conductance of the device. The conductance of the SET can be controlled by varying the tunnel junction width of the SET. Characterization of the SET device is possible by understanding the effect of process parameters on the device parameters of the system. Hence, the design of SETs for different applications would be possible. Also, the design and realization of nano systems incorporating multi functionality in the same module can be made possible. By virtue of their considerably reduced weight and order of magnitude higher speed than the current devices, these nano systems promise to provide revolutionary new capabilities to the Soldiers and the decision makers in the field.

ACKNOWLEDGEMENT

The research reported in this document/presentation was performed in connection with contract DAAD17-03-C-0115 with the U.S. Army Research Laboratory. The views and conclusions contained in this document/presentation are those of the authors and should not be interpreted as presenting the official policies or position, either expressed or implied, of the U.S. Army Research Laboratory or the U.S. Government unless so designated by other authorized documents. Citation of manufacturer's or trade names does not constitute an official endorsement or approval of the use thereof. The U.S. Government is authorized to reproduce and distribute reprints for Government purposes notwithstanding any copyright notation hereon.

REFERENCES

D. Chouvaev and L. S. Kuzmin, D. S. Golubev, A. D. Zaikin, "Strong tunneling and Coulomb blockade in a single-electron transistor," *Phys. Rev. B* **59**(16), pp.10599–10602, 1999.

D. S.Golubev, A. D. Zaikin, "Strong electron tunneling through mesoscopic metallic grains," *Phys. Rev. B* **56**(24), pp. 15782–15792, 1997.

P. Santosh Kumar Karre, Paul L. Bergstrom, Govind Mallick, and Shashi P. Karna, "Single Electron Transistor Fabrication sing Focused Ion Beam Direct Write Technique," *Digest 17th Annual SEMI/IEEE Advanced SemiconductorManufacturing Conference (ASMC2006),* pp. 257 – 260, Boston, MA, 21–24 May 2006.

K. Nakazato, T. J. Thornton, J. White, and H. Ahmed, "Single-electron effects in a point contact using side-gate in delta-doped layers," *Appl. Phys. Lett.* **61**, pp. 3145–3147, 1992.

J. Park and P. L. McEuen, "Formation of a p-type quantum dot at the end of an n-type carbon nanotube," *Appl. Phys. Lett*, **79**, pp. 1363–1365, 2001.

D. Petit and C. C. Faulkner, S. Johnstone, D. Wood, R. P. Cowburn, "Nanometer scale patterning using focused ion beam milling," *Rev. Sci. Instr.* **76**, 026105, 2005.

Y. Takahashi, M. Nagase, H. Namatsu, K.Kurihara, K. Iwadate,Y. Nakajima, S. Horiguchi, K. Murase, and M. Tabe, "Fabrication technique for Si single-electron transistor operating at room temperature," *Elect. Lett.* **31**, pp. 136–137, 1995.